# Analysis 2DWPU core

This variant of the core allows to analyze details of the execution of the core with possibility to alter various parameters, like data throughputs of various memories, latency of several devices and enable simulation of caches.

Each device has a specified data troughput - how many cycles are required for one data retrieval or write. This is achieved by specifying the frequency of the processor core itself and the devices, as well as cycle latency of various devices in the processor. These values are then used to calculate whether a value can be transferred or not – if the required memory troughput is higher than the memory speed, then the processor needs to wait, causing a slow down. This can be analyzes, as the core determines how many cycles the core waited for memory and other units.

## Difference between full core and additional core – separate classes?

There should be only one class, at whether core is full or not is determined by a specific bit in the SW register.